Appl. No. 09/927,695
Amdt. dated May 5, 2003
Reply to Office Action of Feb. 4, 2003

REMARKS

Favorable reconsideration and allowance of the claims of the present application are respectfully requested.

Claims 31-47 stand rejected under 35 U.S.C. §112, second paragraph, as allegedly indefinite for failing to particularly point out and distinctly claim the subject matter which the applicants regard as the invention.

In response thereto, Claim 31 has been amended to include proper antecedent basis. Applicants submit the §112 rejection of Claim 31 has been obviated in light of currently amended Claim 31. Claim 31 has also been amended to positively recite that the oxygen source layer, "is a metal oxide having the formula MO_x, where M is a noble metal, a non-noble metal or mixtures and alloys thereof and x is from about 0.03 to about 3". Support for the amendment to Claim 31 is found in original Claim 39 and also throughout the originally submitted specification; see, i.e., Page 15, line 29- Page 16, line 28.

Claim 34 has been amended to be dependent on newly added Claim 42, which provides proper antecedent basis for a "conductive counterelectrode". Applicants submit that the §112 rejection of Claim 34 has been obviated in light of newly added Claim 48 and currently amended Claim 34.

New Claim 42 clearly and positively recites, "where said ferroelectric capacitor further comprises a conductive electrode layer." Support for new Claim 42 is found throughout the originally submitted application; i.e., Page 12, line 12- Page 15, line 27, and FIGS. 1(b)-1(c).

Insofar as Claim 46 is concerned, applicants have rewritten that claim as independent Claim 49 including the limitation of base Claim 31.

Since the above amendments to the claims do not introduce any new matter into the application, entry thereof is respectfully requested.

Claims 31-42, 45, and 47 stand rejected under 35 U.S.C. §103(a) as allegedly obvious over the publication to Robert E. Jones Jr., *Ferroelectric Nonvolative Memories for Embedded Applications*, IEEE Custom Integrated Circuits Conference (1988)("Jones Jr., et al.") in view of U.S. Patent No. 6,015,989 to Horikawa, et al. ("Horikawa, et al."). Claims 43-44 stand rejected, under 35 U.S.C. §103(a), as allegedly obvious over the combination of Jones Jr., et al., Horikawa, et al., and U.S. Patent No. 6,322,849 to Joshi, et al. ("Joshi, et al.").

Applicants provide a ferroelectric (FE) capacitor and a method of fabricating the same. More specifically, the present invention relates to a method of fabricating an integrated ferroelectric/CMOS structure comprising the steps of: forming at least one complementary metal oxide semiconductor (CMOS) device on a semiconductor wafer; forming a ferroelectric capacitor over said CMOS device, where the ferroelectric capacitor comprising at least a ferroelectric layer 22 and an oxygen source layer 26 in proximity to a conductive electrode layer 20, where said oxygen source layer 26 is a metal oxide having the formula MO_x, where M is a noble metal, a non-noble metal or mixtures and alloys thereof and x is from about 0.03 to about 3, and is capable of at least partially decomposing at temperatures below 700°C; then forming wiring levels 32 on the ferroelectric capacitor at temperatures below 450°C; and annealing the structure at a temperature between 300°C and 700°C so as to at least partially decompose the oxygen source layer to release oxygen into the ferroelectric capacitor. The atomic percent of oxygen in the oxygen source layer, having the formula MO_x where x is from about 0.03 to about 3, is from about 1.5% to about 25%.

Applicants submit that the applied references do not render the claims of the present application obvious because the applied references fail to teach or suggest applicants' claimed method. More specifically, the applied references fail to teach or suggest a method including the step of "forming a ferroelectric capacitor over said CMOS device, said ferroelectric capacitor comprising at least a ferroelectric layer and an oxygen source layer in proximity to a conductive electrode layer, where said oxygen source layer is a metal oxide having the formula MO_x, where M is a noble metal, a non-noble metal or mixtures and alloys thereof and x is from about 0.03 to about 3, and is capable of at least partially decomposing at temperatures below 700°C", as recited in amended Claim 31.

Jones Jr., et al., fail to teach or suggest a method including the step of depositing a oxygen source layer, where the oxygen source layer is a metal oxide having the formula MO_x, where x is from about 0.03 to about 3. Applicants note that the Examiner has admitted in the present Office Action that, "Jones Jr., et al., does not specifically show forming the oxygen source layer in proximity to a conductive electrode layer and releasing oxygen from the oxygen source layer". Therefore, since Jones Jr., et al. fail to teach or suggest an oxygen source layer, Jones Jr., et al. also fail to teach or suggest where the oxygen source layer is a metal oxide having the formula MO_x, where x is from about 0.03 to about 3, as recited in amended Claim 31.

Horikawa, et al. fail to fulfill the deficiencies of Jones Jr., et al. since the applied secondary reference also fails to teach or suggest a method which forms the claimed oxygen source layer, where the oxygen source layer is a metal oxide having the formula MO_x, where x is from about 0.03 to about 3. Horikawa, et al. disclose a semiconductor device having a lower capacitor electrode **130** connected electrically with the major surface of the

semiconductor substrate **101** through the connecting member **110a**; a capacitor dielectric film **115** formed on the lower capacitor electrode **130**; an upper capacitor electrode **116** formed on the capacitor dielectric film **115**; and a second interlayer insulating film **117** formed on the capacitor upper electrode **116**. The lower capacitor electrode **130** is made of a principal component selected from the group consisting of ruthenium and iridium and contains oxygen in a quantity of 0.001 to 0.1% by atomic weight %.

Horiwaka, et al. fail to teach forming an oxygen source layer having the formula MO_x, where x is from about .03 to about 3, because the oxygen concentration of the lower capacitor electrode disclosed in the Horiwaka, et al., is not within the oxygen concentration of applicants' oxygen source layer. In the claimed method, the source layer has the formula MO_x where x ranges from 0.03 to 3. This correlates to an oxygen content of from about 1.5 to about 25 atomic %. The lower capacitor electrode **130** disclosed in Horiwaka, et al. contains oxygen in a quantity of 0.001 to 0.1% by atomic weight %. Horiwaka, et al. thus provides a structure in which the oxygen content is over an order of magnitude lower than the oxygen content in the claimed method. Therefore, Horiwaka, et al. fail to teach or suggest a method step of forming a ferroelectric capacitor over said CMOS device, said ferroelectric capacitor comprising at least a ferroelectric layer and an oxygen source layer in proximity to a conductive electrode layer, where said oxygen source layer is a metal oxide having the formula MO_x, where M is a noble metal, a non-noble metal or mixtures and alloys thereof and x is from about 0.03 to about 3, and is capable of at least partially decomposing at temperatures below 700°C", as recited in amended Claim 31.

Applicants note that Horiwaka, et al. make a single reference to a lower capacitor electrode having an oxygen concentration of about 2% during initial anneal process steps.

See Column 9, lines 24-37. Applicants submit that this reference is to an intermediate process step, where ultimately the lower capacitor electrode is further annealed until the oxygen concentration of the lower capacitor electrode is within the desired range of 0.001 to 0.1 atomic %, as disclosed in Horiwaka, et al. See Column 9, lines 29-34. Therefore, Horiwaka, et al. do not teach or suggest forming an oxygen source layer is a metal oxide having the formula MO_x, where x is from about 0.03 to about 3.

Applicants further submit that Horiwaka, et al. teach away from the present invention. Horiwaka, et al. disclose that a low concentration of oxygen in the lower capacitor electrode suppresses the diffusion of Si in order to reduce the formation of a silicide on the lower electrode. Horiwaka, et al., referring to Column 8, lines 10-25, further disclose that it is disadvantageous, "if the oxygen content in the ruthenium thin-film is increased to a value not lower than 0.05%, it appears that the use of the annealing temperature of 650°C may result in increase of the contact resistance by 2 to 3 units. This appears because the oxygen added to the ruthenium thin-film becomes excessive". A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. W.L. Gore and Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983). Therefore, Horiwaka, et al. teach away from applicants' claimed method as recited in amended Claim 31.

Joshi, et al. also fail to fulfill the deficiencies of the applied prior art. More specifically, Joshi, et al. do not teach or suggest forming an oxygen source layer, where the oxygen source layer is a metal oxide having the formula MO_x, where x is from about 0.03 to about 3. Joshi, et al. provide a method for fabricating a ferroelectric integrated circuit that reduces or eliminates the degradation of electronic properties resulting from exposure to

hydrogen. Joshi, et al., referring to FIG. 1, disclose a ferroelectric capacitor 118 comprising a bottom electrode 120 made of platinum and having a thickness of 2000Å, a ferroelectric thin film 122 formed on the bottom electrode 120, and a top electrode 124 formed on the ferroelectric film 122, made of platinum and having a thickness of 2000 Å. Joshi, et al. do not teach or suggest a method including the step of "forming a ferroelectric capacitor over said CMOS device, said ferroelectric capacitor comprising at least a ferroelectric layer and an oxygen source layer in proximity to a conductive electrode layer, where said oxygen source layer is a metal oxide having the formula MO_x, where M is a noble metal, a non-noble metal or mixtures and alloys thereof and x is from about 0.03 to about 3" as recited in amended Claim 31.

The §103 rejections also fail because there is no motivation in the applied references which suggests modifying the disclosed methods and structures to include the various features, particularly the claimed method including forming a ferroelectric capacitor over said CMOS device, said ferroelectric capacitor comprising at least a ferroelectric layer and an oxygen source layer in proximity to a conductive electrode layer, where said oxygen source layer is a metal oxide having the formula MO_x, where M is a noble metal, a non-noble metal or mixtures and alloys thereof and x is from about 0.03 to about 3. Thus, there is no motivation provided in the applied references, or otherwise of record, to make the modification mentioned above. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Vaeck, 947 F.2d, 488, 493, 20 USPQ 2d. 1438, 1442 (Fed.Cir. 1991).

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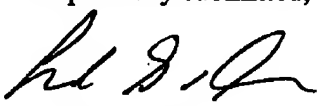
The rejections under 35 U.S.C. §103 have been obviated; therefore reconsideration and withdrawal thereof are respectfully requested.

Thus, in view of the foregoing amendments and remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,



Leslie S. Szivos
Registration No. 39,394

Scully, Scott, Murphy & Presser
400 Garden City Plaza
Garden City, New York 11530

HAH/LSS:gc